IN THE CLAIMS:

Claims 2 and 16 have been amended herein. All of the pending claims 1 through 22 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

1. A method for preparing a surface of a semiconductor device structure for planarization, comprising:

providing a semiconductor device structure including at least one recess formed in a surface thereof and a first material layer substantially filling said at least one recess and covering said surface, said first material layer having a nonplanar surface;

applying a second material to said first material layer; and

spreading said second material over said first material layer so as to form a second material layer having a substantially planar surface without requiring subsequent planarization of said second material.

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2. (Amended) The method of claim 1, wherein said applying said second material comprises applying a stress buffer material to said first material layer.

3. The method of claim 1, wherein said spreading comprises:

spinning said semiconductor device structure at a first speed;

gradually decreasing a rate of said spinning to a second speed; and

gradually increasing a rate of said spinning to a third speed.

4. The method of claim 3, wherein spinning said semiconductor device structure at said second speed comprises permitting said second material within said at least one recess to at least partially set.

5. The method of claim 3, wherein spinning said semiconductor device structure at said third speed comprises forming said second material over said surface to a desired thickness.

6. The method of claim 1, wherein said providing comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure.

7. The method of claim 6, wherein said providing further comprises providing said shallow trench isolation structure with said first material layer comprising an electrical insulator material.

8. The method of claim 1, wherein said providing comprises providing a semiconductor device structure with said at least one recess comprising at least one dual damascene trench formed therein.

9. The method of claim 8, wherein said providing further comprises providing a semiconductor device structure with said first material layer comprising conductive material.

10. The method of claim 2, wherein said spreading comprises at least partially filling at least one valley of said first material layer with said stress buffer material while leaving at least one peak of said first material layer substantially uncovered by said stress buffer material.

11. The method of claim 10, further comprising planarizing at least said first material layer.

12. The method of claim 11, wherein said planarizing comprises etching at least one region of said first material layer exposed through said stress buffer material with selectivity over said stress buffer material.

13. The method of claim 12, wherein said etching is effected until a surface of said at least one region is in substantially the same plane as a surface of said stress buffer material.

14. The method of claim 13, wherein said planarizing further comprises abrasively planarizing said stress buffer material and said at least one region to expose said surface of said semiconductor device structure adjacent said at least one recess, said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing.

15. The method of claim 13, wherein said planarizing further comprises concurrently etching said first material layer and said stress buffer material at substantially the same rate so as to expose said surface of said semiconductor device structure adjacent said at least one recess with said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing.

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16. (Amended) The method of claim 11, wherein said planarizing is effected until said surface of said semiconductor device structure is exposed through said first material layer.

17. The method of claim 16, wherein said etching is effected until a surface of said first material layer in said at least one recess is in substantially the same plane as said surface of said semiconductor device structure.

18. The method of claim 16, further comprising removing said stress buffer material from said semiconductor device structure.

19. The method of claim 2, wherein said spreading comprises forming a substantially planar surface over said semiconductor device structure.

20. The method of claim 19, further comprising planarizing at least said first material layer.

21. The method of claim 20, wherein said planarizing comprises substantially concurrently abrasively planarizing said stress buffer material and said first material layer to expose said surface of said semiconductor device structure adjacent said at least one recess, said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing.

22. The method of claim 20, wherein said planarizing comprises substantially concurrently etching said first material layer and said stress buffer material at substantially the same rate so as to expose said surface of said semiconductor device structure adjacent said at least one recess with said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing.